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EXAMINER	
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ART UNIT	PAPER NUMBER
2186	12

DATE MAILED: 04/20/01

Below is a communication from the EXAMINER in charge of this application

COMMISSIONER OF PATENTS AND TRADEMARKS

ADVISORY ACTION

☑ THE PERIOD FOR RESPONSE:

a) ☐ is extended to run _____ or continues to run _____ from the date of the final rejection

b) ☑ expires three months from the date of the final rejection or as of the mailing date of this Advisory Action, whichever is later. In no event however, will the statutory period for the response expire later than six months from the date of the final rejection.

Any extension of time must be obtained by filing a petition under 37 CFR 1.136(a), the proposed response and the appropriate fee. The date on which the response, the petition , and the fee have been filed is the date of the response and also the date for the purposes of determining the period of extension and the corresponding amount of the fee. Any extension fee pursuant to 37 CFR 1.17 will be calculated from the date of the originally set shortened statutory period for response or as set forth in b) above.

☐ Appellant's Brief is due in accordance with 37 CFR 1.192(a).

☑ Applicant's response to the final rejection, filed 3/29/01 has been considered with the following effect, but it is not deemed to place the application in condition for allowance:

1. ☑ The proposed amendments to the claim and /or specification will ~~not~~ be entered and the final rejection stands because:

   a. ☐ There is no convincing showing under 37 CFR 1.116(b) why the proposed amendment is necessary and was not earlier presented.

   b. ☐ They raise new issues that would require further consideration and/or search. (See Note).

   c. ☐ They raise the issue of new matter. (See Note).

   d. ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal.

   e. ☐ They present additional claims without cancelling a corresponding number of finally rejected claims.

NOTE: Applicant's arguments have been considered; however they are not overcomed the Final Rejection. In addition, it should be noted that the OFFICIAL Notice cited to support the basic concept of Cache operation (as indicated in the Final action, page 9), Jim Handy clearly supports the cache entries include a tag portion, match detection logic for tag portion to generate cache/hit, miss. See further attached response.

2. ☐ Newly proposed or amended claims _____ would be allowed if submitted in a separately filed amendment cancelling the non-allowable claims.

3. ☐ Upon the filing an appeal, the proposed amendment ☐ will be entered ☐ will not be entered and the status of the claims will be as follows:

   Claims allowed: _____
   Claims objected to: _____
   Claims rejected: _____

   However;

   ☐ Applicant's response has overcome the following rejection(s): _____

4. ☑ The ~~affidavit, exhibit or~~ request for reconsideration has been considered but does not overcome the rejection because of the reasons & examples given in the NOTE & attached response.

5. ☐ The affidavit or exhibit will not be considered because applicant has not shown good and sufficent reasons why it was not earlier presented.

☐ The proposed drawing correction ☐ has ☐ has not been approved by the examiner.

☑ Other See attached response & PTO-892

PTOL-303 (REV. 5-89)

RESPONSE TO AMENDMENTS

1. This action is responsive to communication filed on March 29, 2001.

2. The Information Disclosure Statement filed March 29, 2001 fails to comply with provisions of MPEP 609 because it has been filed after the final rejection mailed February 26, 2001 (paper #9) which requires (a) Certification; (b) Petition and (c) Rule 1.17(i)(1) petition fee. It has been placed in the application file for record.

3. With respect to the remark, first of all, as mentioned in the final rejections that "With regards to other basic concept of cache operation that being omitted in the specification of Chittor *wherein cache entries include a tag portion, match detection logic for tag portion to generate cache hit/miss depending on the results of the detection* (emphasis added), Examiner wholeheartly believes the invention of Chittor does anticipate those limitations, and Examiner hereby takes Official Notice of those limitations, and gladly provide further information upon requests by Applicant's counsel. With that, Examiner would like to direct Applicant's Counsel to Jim Handy, section 1.5; CACHE DATA AND CACHE-TAG MEMORIES, also section 2.1.3, figures 2.4-2.6 and pages 44-46, wherein the concept of

cache hit/miss, cache-tag directory, CAM, generating cache hit/miss signal depending on the results of the detection is clearly described therein. Specifically, in figures 2.4, Jim Handy clearly laid out different scenarios of cache read hit cycle, cache read miss cycle, cache write hit cycle and cache write miss cycle with cache data memory having plurality of entries, and cache tag directory associated with cache data memory. Therefore, Jim Handy reference clearly provides valid and sufficient supports for the Official Notice taken in the final rejection by Examiner. With regard to claim 17, in which it claims "a method of processing a data request with a processing agent comprising posting the data request internally with the agent, determining whether the request hit the cache, when the request misses the cache, posting a sequence of external transactions to fill a cache line with data associated with the data request.". Examiner would like to emphasize that these steps are taught by Chittor to the extent that they are being claimed, and further supported by the Official Notice cited by Examiner during the interview; for example, Jim Handy (pages 79-82), figure 2.22(a) shows that when CPU request either a data read or write, the request is being posted to the address register, and determining whether the hit or miss, and if miss is detected, (loading main memory data into line buffer and CPU, outputting dirty line's tag bits, address register's set bits and

data RAM'S dirty data to main memory, and write line buffer data into tag and data RAMs); also see section 4.2, 4.2.2 for maintaining coherency in Multiple logical caches in Multiprocessor System. In addition, the concept of "filling a cache with data associated with the requested data when there is a miss" is notorious and known in the cache memory storage design; Chittor discloses multiple agents 10-40 each including a cache 14, and the agent 50 which includes MIOC 100 and system memory 200, wherein MIOC cooperates with other agents to **EXCHANGE** ***data between the memory 200 and data caches of the agents*** (emphasis added) which clearly embeds the operation of filling the agent local caches with the requested data (either from the system memory 200 or other caches) when there is a cache miss occurs at that particular requested agent. Chittor's column 5, line 61 bridging column 6, line 12 further discloses that "if the pipelined bus transaction is a read request, the bus request decoder 124 receives the requested data from the pipelined bus and stores it in the staging buffer 160. If the request is a read invalidate transaction, the bus request decoder 124 causes a memory controller 190 to fetch data of the cache line from the memory subsystem 200 and store it in the staging buffer 160. The bus request decoder 124 also observes cache coherency signaling on the pipelined bus 60. If the cache coherency results indicate modified data present in another agent, the bus request decoder

124 causes the memory controller 190 to discontinue fetching of the data. ***The data instead is received by the bus request decoder 124 from the pipelined bus 60 and stored in the staging buffer 160***. When the pipelined bus transaction is complete, the outbound transaction queue 150 stores transaction information and the staging buffer 160 stores an entire cache line of data. To generate the response message on the serial bus 70, the requested data is read from the cache line and placed in a response message.". With regard to the limitations being contended by Applicant that being omitted in the action wherein: cache entries include a tag portion to stored address information, match detection logic for tag portion, control logic provided in communication with match detection logic, signal lines including a cache hit and a tag hit signal line, comparing address information of the data request with tags stored in the cache, and identifying cache miss with the information does not match any stored tag (embedded in basic cache structure of Chittor and shown in Handy's section 1.5, and figure 2.4); the total number of address and status entries equal to the number of data line length provided in the cache entries, Chittor discloses the inbound transaction queue 130 holds information pertaining to the address of the transaction as well as the status information with respect to each line in the cache (figure 1).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is 703-305-3842.

The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Matthew M. Kim can be reached on (703) 308-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TVT/April 14, 2001

Tuan V. Thai

PRIMARY EXAMINER

Group 2100